

PCIe® Electrical Update

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Disclaimer

The information in this presentation refers to specifications still in the development process. This presentation reflects the current thinking of various PCI-SIG® workgroups, but all material is subject to change before the specifications are released.

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Outline

- **PCIe® 5.0 Overview and Signaling Decision**
- **Major 5.0 Electrical Changes**
 - Channel Budget
 - Reference Equalizer
 - Precoding
 - PLL Bandwidth and Model CDRs
 - Tx Jitter Budget at 8 and 16 GT/s
 - Rx Stressed Eye Methodology and FEXT/NEXT Rx Test Modes
- **Lane Margining**

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PCIe 5.0 Overview

- **Key attributes of PCIe 5.0**
 - 32 GT/s NRZ, using scrambling, same as 8/16 GT/s
 - Physical layer BER target remains E-12 (no FEC)
 - Maintains full backward compatibility – including mechanical with installed base of PCIe devices
 - Limited channel reach:
 - Approx. 10” one connector (including 3-4” add-in card) for ~ 2.0 dB/inch FR-4
 - Approx. 16-20” one connector (including 3-4” add-in card) for Meg-6
 - Long channels require retimers or lower loss channels

- **New features**
 - Precoding
 - Common SRIS and CC model CDRs
 - Revised CC CDR and PLL Bandwidth specifications – retroactively applied to 8 and 16 GT/s
 - FEXT/NEXT RX Test Modes

- **This presentation focuses on items changed relative to the PCIe 4.0 specification**
 - Transmitter
 - Receiver
 - Channel
 - Reference Clock

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25 vs 32 GT/s NRZ Pathfinding Key

	No identified issues – no significant issues expected
	Minor issues or differences vs 25 GT/s – not believed to be significant
	Major issues – believed solvable (if necessary)
	Major issue(s) – do not believe they can be solved

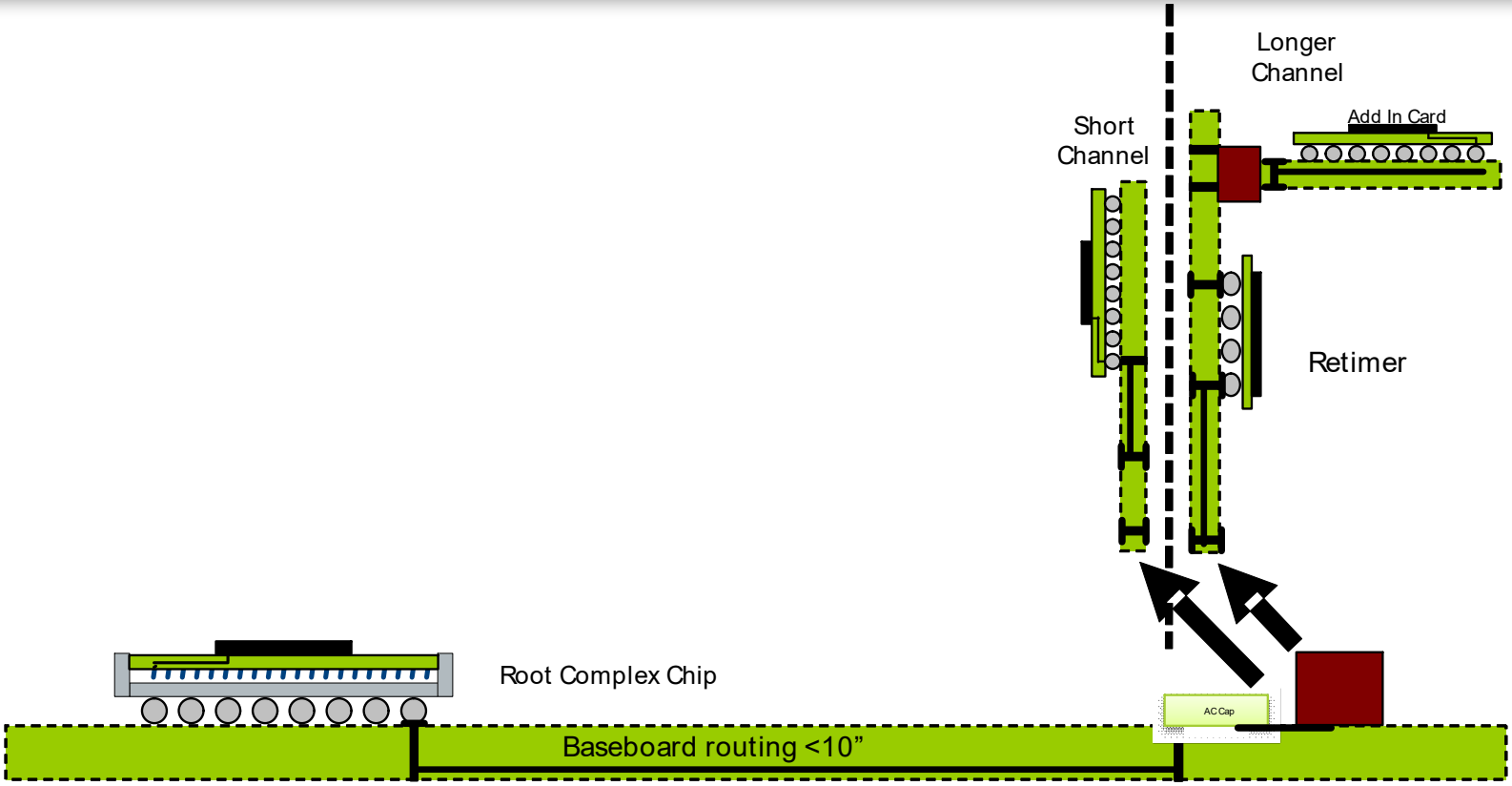
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Pathfinding Summary

	25 GT/s	32 GT/s
Reference Clock		
Retimer		
Silicon Power (pj/bit)		10% type addition vs 25 GT/s per average opinion
Silicon Area See straw poll slide TBD		
Connector - SMT		
Connector – PTH (not needed?)		
Time to 1.0 Spec – 30 – 35 dB (pad to pad)		
Channel Reach Without Retimer– 30 dB (pin to pin reach)	FR-4 (2.0 scaled) 9.9” Meg-4 (1.5 scaled) 13.2” Meg-6 (1.0 scaled) 17.8”	FR-4 (2.0 dB/inch) 6.1” Meg-4 (1.5 dB/inch) 8.2” Meg-6 (1.0 dB/inch) 12.3” Likely to need retimers for CEM
Channel Reach Without Retimer – 35 dB (pin to pin reach)	FR-4 (2.0 scaled) 13” Meg-4 (1.5 scaled) 17.4” Meg-6 (1.0 scaled) 26”	FR-4 (2.0 dB/inch) 8.6” Meg-4 (1.5 dB/inch) 11.5” Meg-6 (1.0 dB/inch) 17.3”
Test Equipment Readiness	Rx training may not work if required to go to 8 or 16 GT/s before 25 GT/s	
Full Bandwidth 400G Ethernet support with x16	Up to 25% bandwidth shortage	

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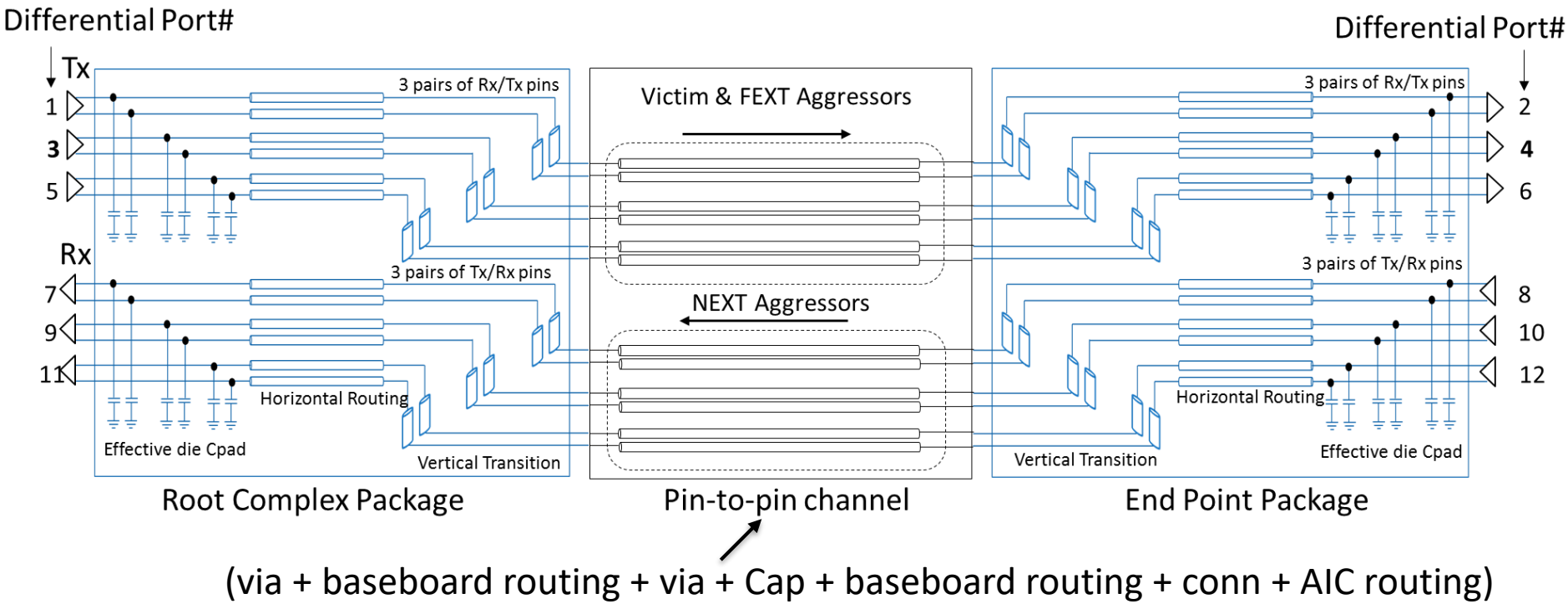
PCI Express® 5.0 Channels



- End to end loss target ~= 36 dB
- Root Package loss ~= 9 dB
- Add-in Card Package loss (Non root) ~= 4 dB
- Total Add-in Card ~= TBD dB
- Connector < 1.5 dB

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Reference Packages



Lane 3->4 is worst-case victim with two Far-end Crosstalk (FEXT) and three Near-end Crosstalk (NEXT) aggressors
Cross-talk Very Important for PCIe 5.0 Channel Simulations

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Minimum 5.0 Target Connector Performance

- Insertion Loss < -1.5 dB to16 GHz
- Cross-talk < -40 dB to 16 GHz
- Return Loss < -10 dB to 16 GHz

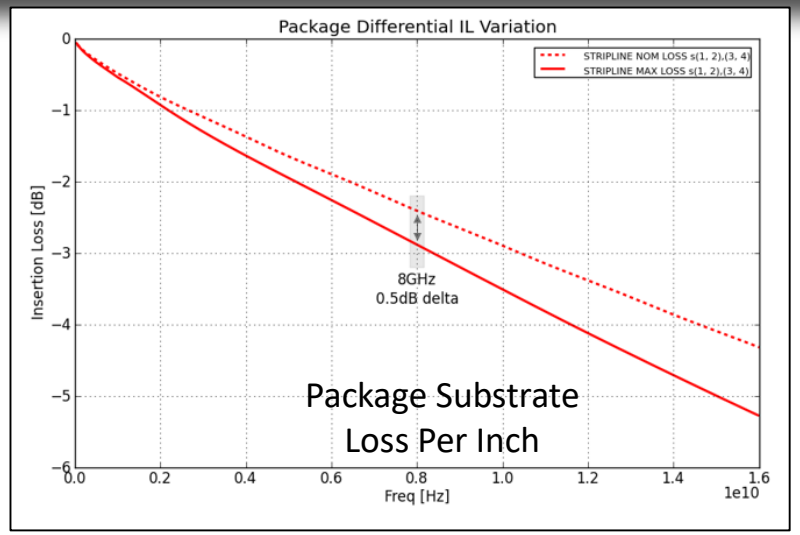
- Signal integrity requirements are normalized to 85 Ohms

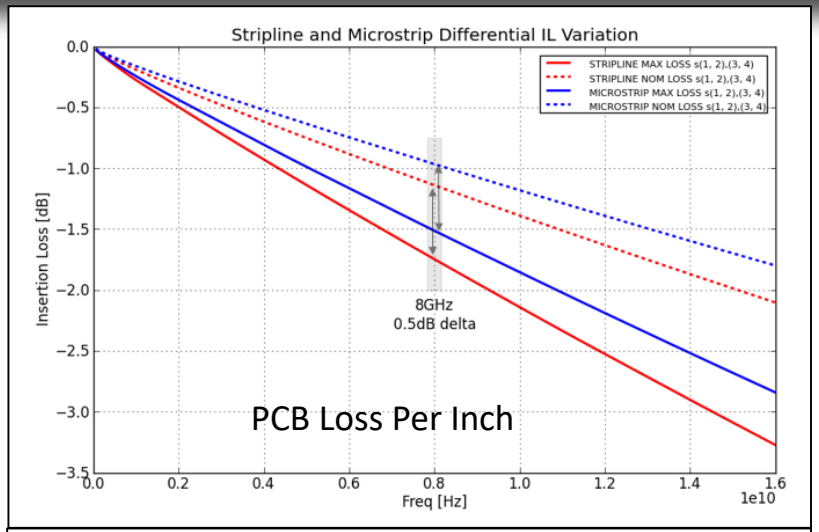
- Assume CEM add-in card gold-finger length can be reduced to at least 3 mm
- Assume there will be some type of small width spike averaging/exclusion that allows small deviations above these targets
- Assume additional motherboard side ground vias could be added

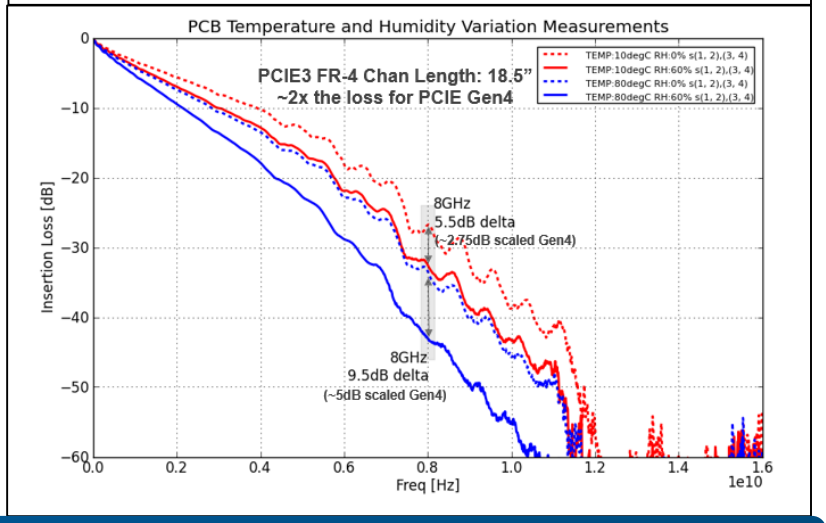
Mechanical Backwards Compatible Solutions Possible

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Channel Loss Over PVT





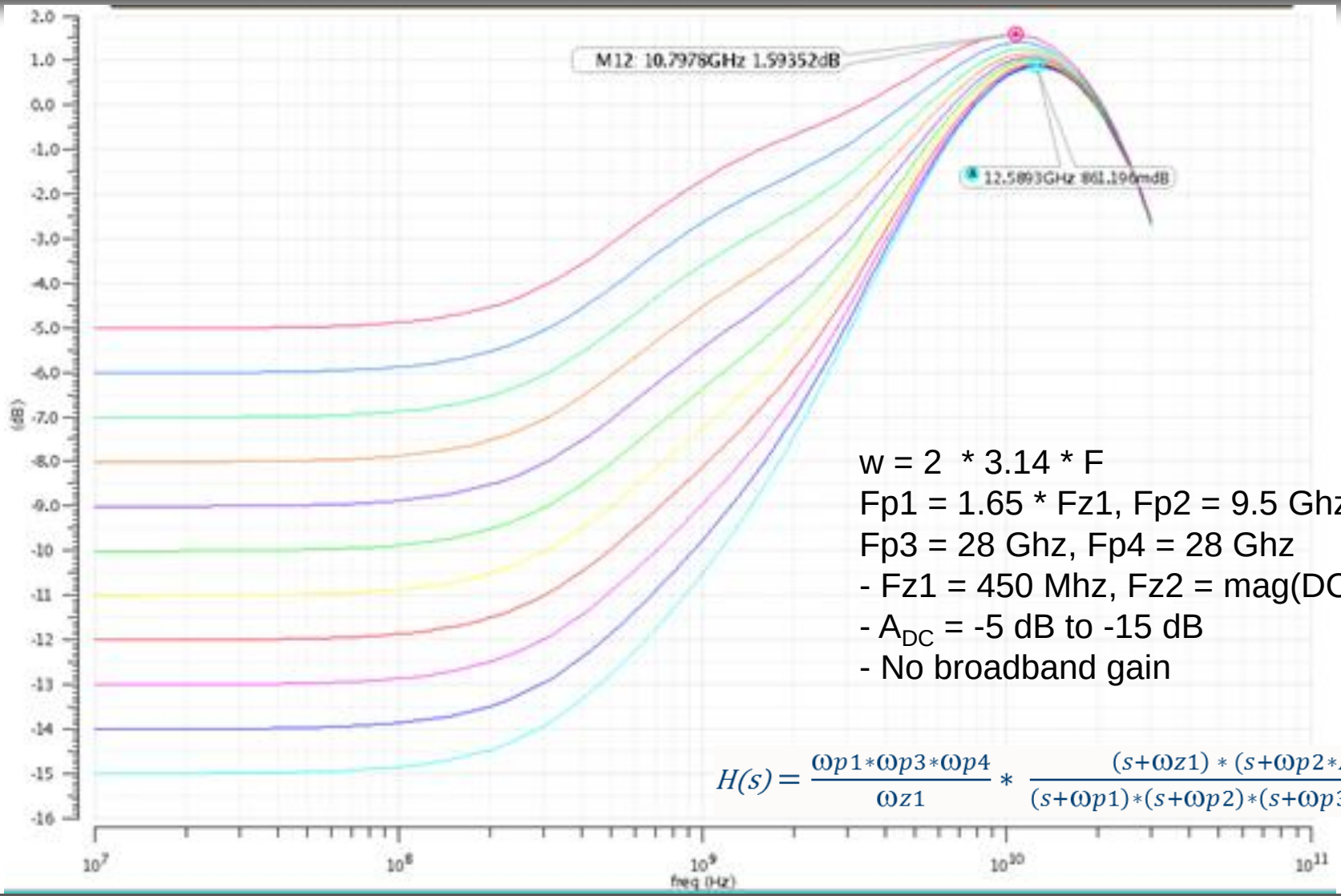


- **Package substrate & PCB loss per inch model used for channel study**
 - Tan delta [0.015 to 0.025]
 - Copper conductivity & roughness
 - Temperature & humidity variation
- **PCIE3 CEM cal channel RH & temp variation measurement @ 8GHz**
 - 12.5" Riser
 - 4" Mainboard
 - 2" CLB

Electrical Specifications Apply Over PVT

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Reference CTLE for 32 GT/s Reference Equalizer



w = 2 * 3.14 * F
Fp1 = 1.65 * Fz1, Fp2 = 9.5 Ghz,
Fp3 = 28 Ghz, Fp4 = 28 Ghz
- Fz1 = 450 Mhz, Fz2 = mag(DC gain)* Fp2
- A_{DC} = -5 dB to -15 dB
- No broadband gain

$$H(s) = \frac{\omega p1 * \omega p3 * \omega p4}{\omega z1} * \frac{(s+\omega z1) * (s+\omega p2 * Adc)}{(s+\omega p1) * (s+\omega p2) * (s+\omega p3) * (s+\omega p4)}$$

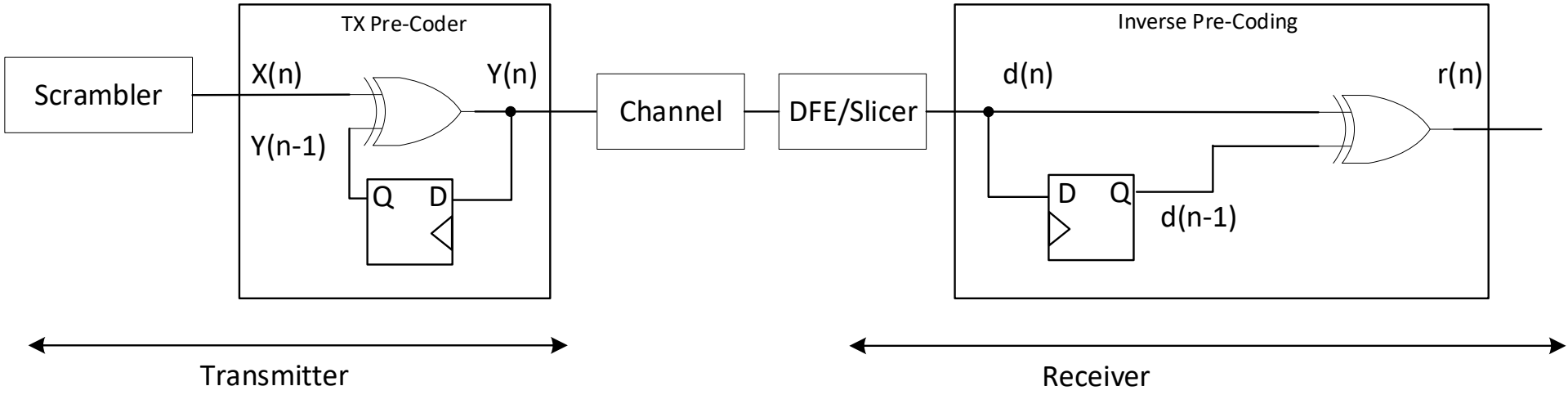
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Behavioral DFE for 32 GT/s

- **3 taps**
- **Benefit of Additional Taps Small for Target Channels With Improved Reference CTLE**
- **Tap 1 Limit is defined as ratio of tap magnitude (h1) to cursor strength (h0)**
 - The h1/h0 limit is 0.8
 - This bounds the reference receiver behavior but does not guarantee that real implementations will be safe from error burst from large h1/h0 causing undetected data corruption
 - Pre-coding added to help mitigate risk of undetected data corruption with large h1/h0 ratios in real implementations
- **Taps 2 and 3 have +/- 20 mV limit**

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Selectable Pre-Coding



- **TX implements the pre-coder**
- **RX implements the Inverse pre-coder**
- **RX can request TX to enable pre-coder in training**
- **Precoding done on all scrambled data**

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Pre-coding Example with Error Burst

Binary bits: X(n)	Precoded Bits: y(n)	Previous Precoded Bits: y(n-1)	Decision Bits: d(n)	Decoded Received Bits: r(n)	Comments
1	1		1		Arbitrary initial value
0	1	1	1	0	
1	0	1	0	1	
0	0	0	0	0	
1	1	0	1	1	
1	0	1	0	1	
0	0	0	0	0	
0	0	0	0	0	
1	1	0	1	1	
0	1	1	1	0	
1	0	1	0 ->1	0	Entry Error
1	1	0	1 ->0	1	Error Corrected
1	0	1	0->1	1	Error Corrected
1	1	0	1->0	1	Error Corrected
0	1	1	1	1	Exit Error
0	1	1	1	0	
1	0	1	0	1	
1	1	0	1	1	
		1			

Burst Error can Continue, but total decoded error is limited to 2-bit errors



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Reference Clock and PLL Bandwidth

Data Rate	CC jitter Limit
2.5 GT/s	86 ps pp
5.0 GT/s	3.1 ps RMS
8.0 GT/s	1.0 ps RMS
16.0 GT/s	0.5 ps RMS
32.0 GT/s	0.15 ps RMS

- Short channel and 50 ohm terminations for reference clock phase jitter measurement
- Lower PLL bandwidth limit for 8 and 16 GT/s reduced to 0.5 MHz
 - Revised model CDR at 16 GT/s for backward compatibility
 - Reduced TX UTJ limit at 8 GT/s for backward compatibility

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
BW_{PLL}(min) = 0.5 MHz	ω_{n1}= .112 Mrad/s ζ_1 = 14	ω_{n1}= 1.51 Mrad/s ζ_1 = 0.73
BW_{PLL}(max) = 1.8 MHz	ω_{n1}= .403 Mrad/s ζ_1 = 14	ω_{n1}= 5.42 Mrad/s ζ_1 = 0.73

32.0 GT/s CC **CDR**

16 combinations

32.0 GT/s

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Transmitter Specification

- **Preset definition**
 - Retain P0-P10 with same definition as PCIe 4.0 at 16 GT/s
- **Package loss (ps21TX equivalent)**
 - Normative for all devices
- **Architecture Specific Post Processing**
 - Common vs. Independent Refclk architectures
- **Jitter parameters**
 - Applied uniformly for all five data rates
- **Return Loss extended up to 16 GHz**
 - T-coils likely required to meet limits
 - Effective pad capacitance in reference package models ~ 200 fF
- **CTLE option for de-embedding breakout channel**

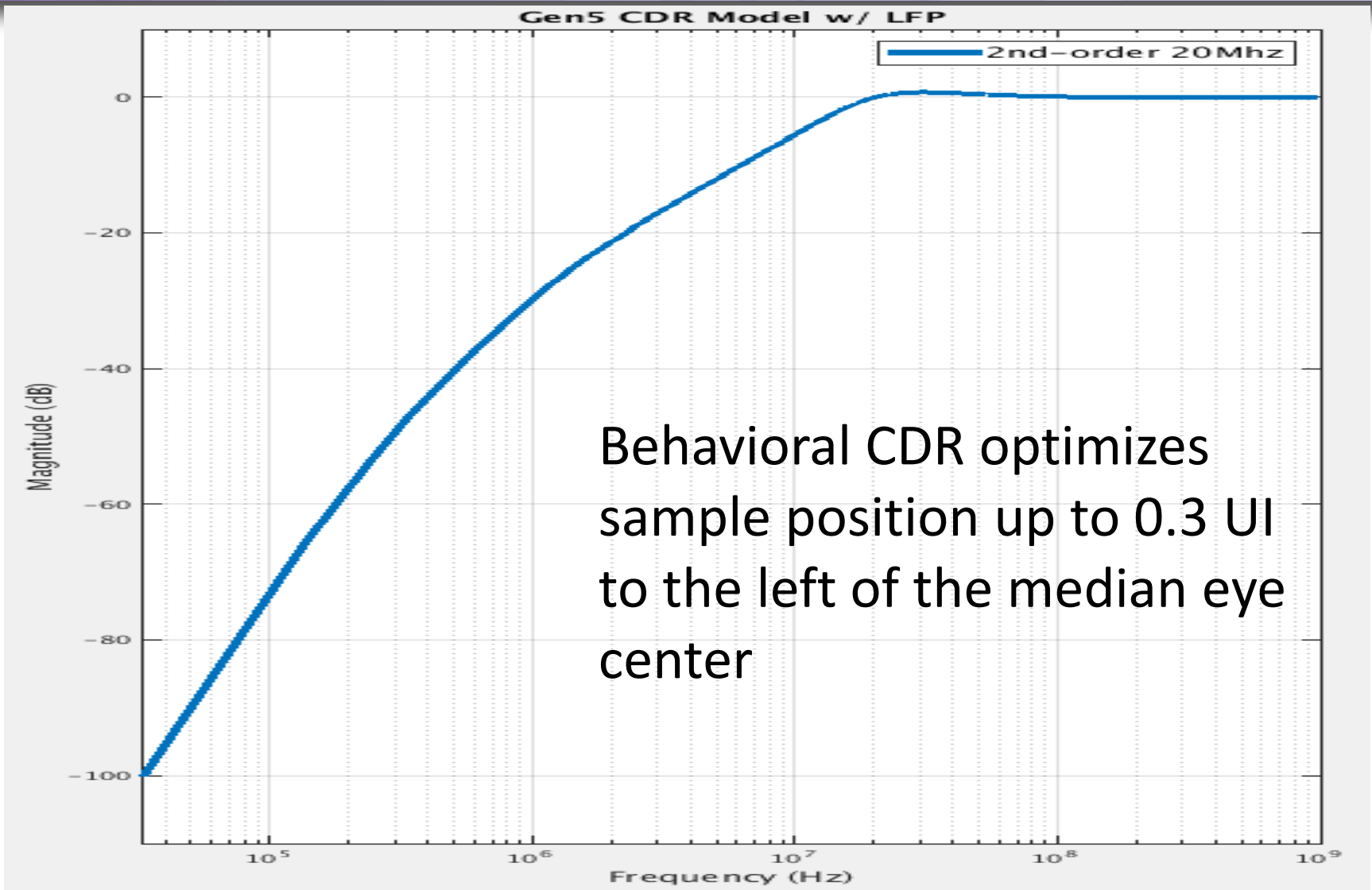
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Transmitter Jitter Requirements

		2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	
T_{TX-UTJ}	Tx uncorrelated total jitter	100 (max)	50 (max)	27.55 (max)	11.8 (max)	6.25 (max)	ps PP at 10^{-12}
$T_{TX-UTJ-SRIS}$	Tx uncorrelated total jitter when testing for the IR clock mode with SSC	100 (max)	66.51 (max)	33.83 (max)	15.85 (max)	7.15 (max)	ps PP at 10^{-12}
$T_{TX-UDJDD}$	Tx uncorrelated Dj for non-embedded Refclk	100 (max)	30 (max)	12 (max)	6.25 (max)	3.125 (max)	ps PP
$T_{TX-UPW-TJ}$	Total uncorrelated pulse width jitter	N/A	40 (max)	24 (max)	12.5 (max)	6.25 (max)	ps PP at 10^{-12}
$T_{TX-UPWDJDD}$	Deterministic DjDD uncorrelated pulse width jitter	N/A	40 (max)	10 (max)	5 (max)	2.5 (max)	ps PP
T_{TX-RJ}	Tx Random jitter	N/A	1.4 – 3.6	1.17 – 1.97	0.40 – 0.84	.23-.45	ps RMS

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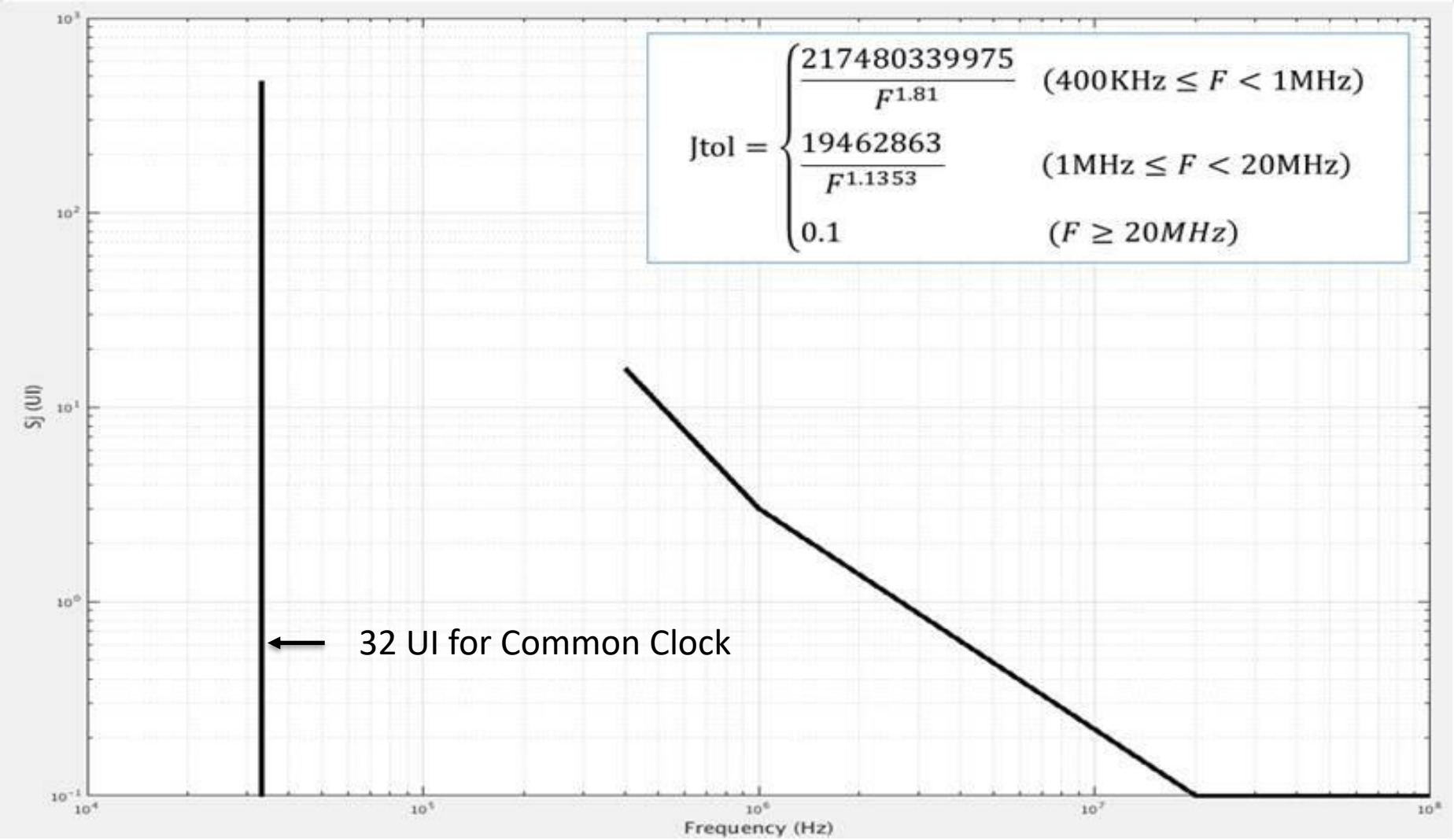
32 GT/s SRIS and CC Model CDR



Behavioral CDR optimizes sample position up to 0.3 UI to the left of the median eye center

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32 GT/s SRIS Jitter Tolerance

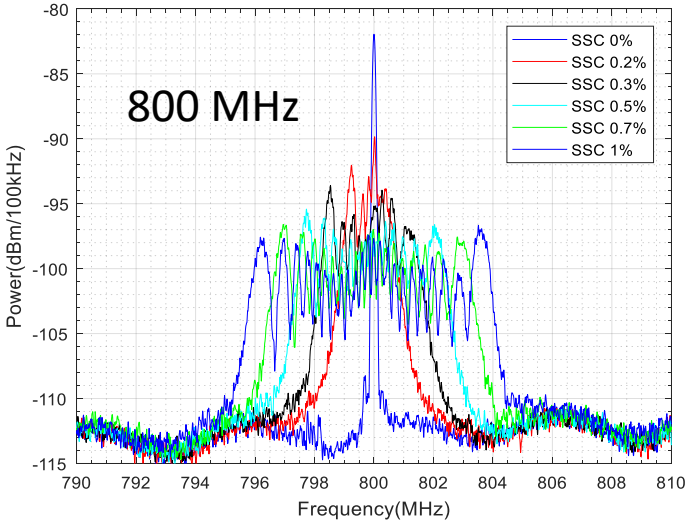


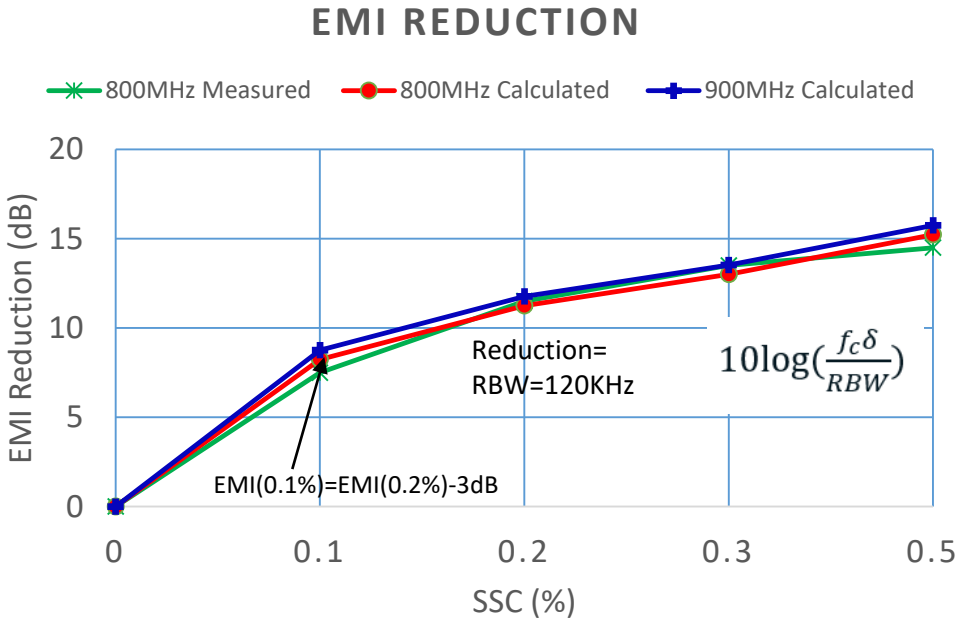
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SRIS – Maximum SSC PPM

EMI (<1GHz; RBW=100Khz) vs. SSC %
(Measured Data from an Actual SOC)

- Spectrum analyzer measurement
- Average detector, 100kHz RBW





PPM	900MHz EMI Benefit Losses from 0.5%
0.3%	~2dB
0.2%	~4dB
0.1%	~7dB
0%	~15dB

5.0 SRIS Maximum SSC PPM Reduced to 3000

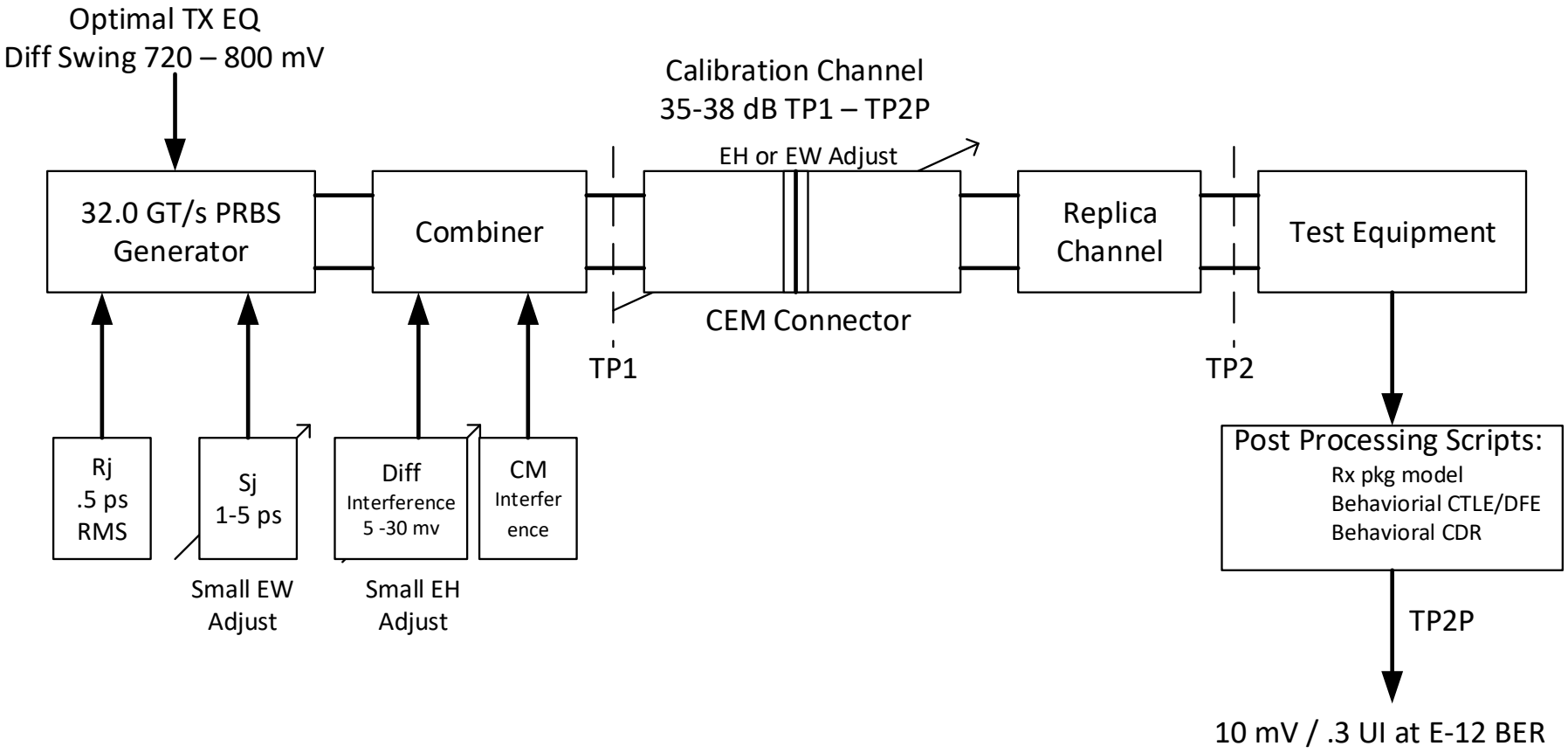
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Receiver Specification

- **Stressed eye methodology applied to all data rates**
 - Stressed jitter and voltage as a single test
- **Calibration channel defined by data rate dependent mask**
 - Direction to make loss variable at 16 and 32 GT/s
 - Minimize Rj/Sj/DM variation across different set-ups
- **Separate Root Complex and AIC behav pkg models**
- **Rx Replica Channel 85 ohm nominal (16 and 32 GT/s)**
- **Behavioral Rx equalization data rate dependent**
 - 2.5 and 5 GT/s: none
 - 8 and 16 GT/s: CTLE and DFE (8G: 1 tap, 16G, 2 taps)
 - 32 GT/s: 2nd order CTLE and DFE (3 taps)
- **Eye height minimum reduced to 10mV for 32G**

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32 GT/s Rx Calibration



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FEXT/NEXT Test Modes

- **Single Lane BERT Can Place Any Lane in Loopback with Phase 2/Phase 3 Tx Equalization Training**
- **All Other DUT Transmitters Can Be Configured For**
 - Transmit Tx Compliance Pattern
 - Tx Electrical Idle
- **All Other DUT Receivers Can Be Configured to Ignore Incoming Data**
- **Allows Potential Base/CEM Rx Testing To Capture Real NEXT and/or FEXT**

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EIEOS Update

- **Base spec requires a min of 175mVpk-pk at RX pin, using Preset10 (9.5dB boost +/-1.5dB)**
- **Rx die pad simulation using example worst-case ~ -36 dB server channel less than 175 with 16 ones and zeros**
- **EIEOS at 32 GT/s only changes to 32 ones and zeros for two consecutive blocks**

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Lane Margining

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Lane Margining Parameters (1)

Parameter Name	Min	Max	Description
$M_{NumTimingSteps}$	6	63	Number of time steps from default (to either left or right), range must be at least +/-0.2UI Timing offset must increase monotonically The number of steps in both positive (toward the end of the unit interval) and negative (toward the beginning of the unit interval) must be identical
$M_{MaxTimingOffset}$	20	50	Offset from default at maximum step value as percentage of a nominal UI at 16.0 GT/s A 0 value may be reported if the vendor chooses not to report the offset
$M_{NumVoltageSteps}$	32	127	Number of voltage steps from default (either up or down), minimum range +/-50mV as measured by 16.0 GT/s reference equalizer Voltage offset must increase monotonically The number of steps in both positive and negative direction from the default sample location must be identical This value is undefined if $M_{VoltageSupported}$ is 0b
$M_{MaxVoltageOffset}$	5	50	Offset from default at maximum step value as percentage of one volt A 0 value may be reported if the vendor chooses not to report the offset when $M_{VoltageSupported}$ is 1b This value is undefined if $M_{VoltageSupported}$ is 0b
$M_{SamplingRateVoltage}$	0	63	The ratio of bits tested to bits received during voltage margining. A value of 0 is a ratio of 1:64 (1 bit of every 64 bits received), and a value of 63 is a ratio of 64:64 (all bits received).
$M_{SamplingRateTiming}$	0	63	The ratio of bits tested to bits received during timing margining. A value of 0 is a ratio of 1:64 (1 bit of every 64 bits received), and a value of 63 is a ratio of 64:64 (all bits received).

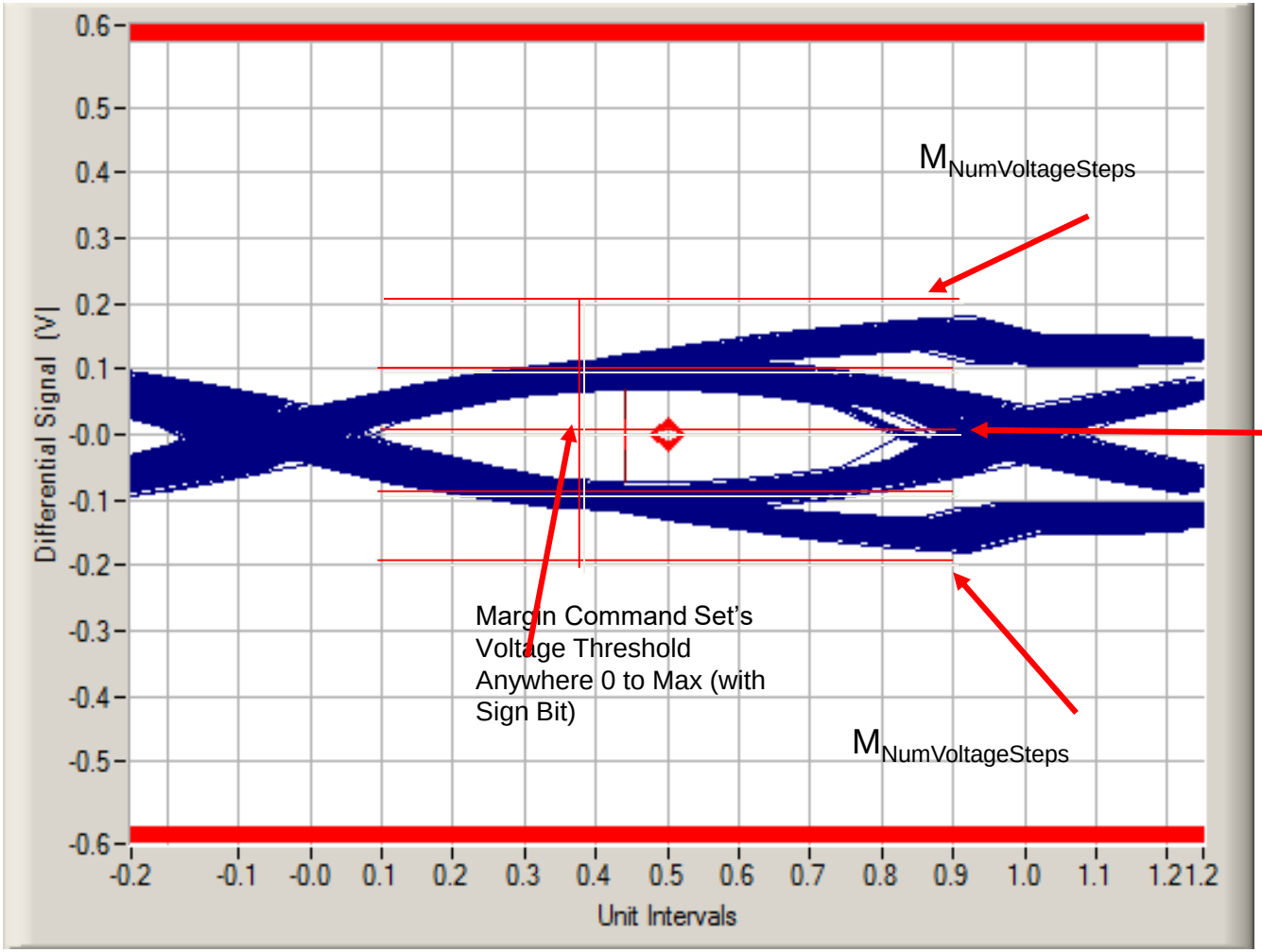
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Lane Margining Parameters (2)

Parameter Name	Min	Max	Description
$M_{VoltageSupported}$	0	1	1b indicates that voltage margining is supported
$M_{IndLeftRightTiming}$	0	1	1b indicates independent left/right timing margin supported
$M_{IndUpDownVoltage}$	0	1	1b independent up and down voltage margining supported
$M_{IndErrorSampler}$	0	1	1b Margining will not produce errors (change in the error rate) in data stream (ie. – error sampler is independent) 0b Margining may produce errors in the data stream
$M_{MaxLanes}$	0	31	Maximum number of Lanes that can be margined at the same time. Recommended that this value is equal to the number of Lanes in the Link Note: This value shall not exceed the number of Lanes in the Link
$M_{SampleReportingMethod}$	0	1	Indicates whether sampling rates ($M_{SamplingRateVoltage}$ and $M_{SamplingRateTiming}$) are supported (1) or a sample count is supported (0). One of the two methods is supported by each device.
$M_{ErrorCount}$	0	63	If $M_{IndErrorSampler}$ is 1b this is a count of the actual bit errors since margining started. If $M_{IndErrorSampler}$ is 0b this is the actual count of the logical errors since margining started. See the Physical Layer chapter for the definition of what errors are counted. 111111b indicates >=63 errors
$M_{SampleCount}$	0	127	Value = 3*log 2 (number of bits margined). Where number of bits margined is a count of the actual number of bits tested during marging. The count resets on new margin command and stops when error count limit is reached or sample count saturates (also stops margining) The count resets to zero when a new margin command is received.

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Voltage Margin Example
Considering Making Voltage Margin Required

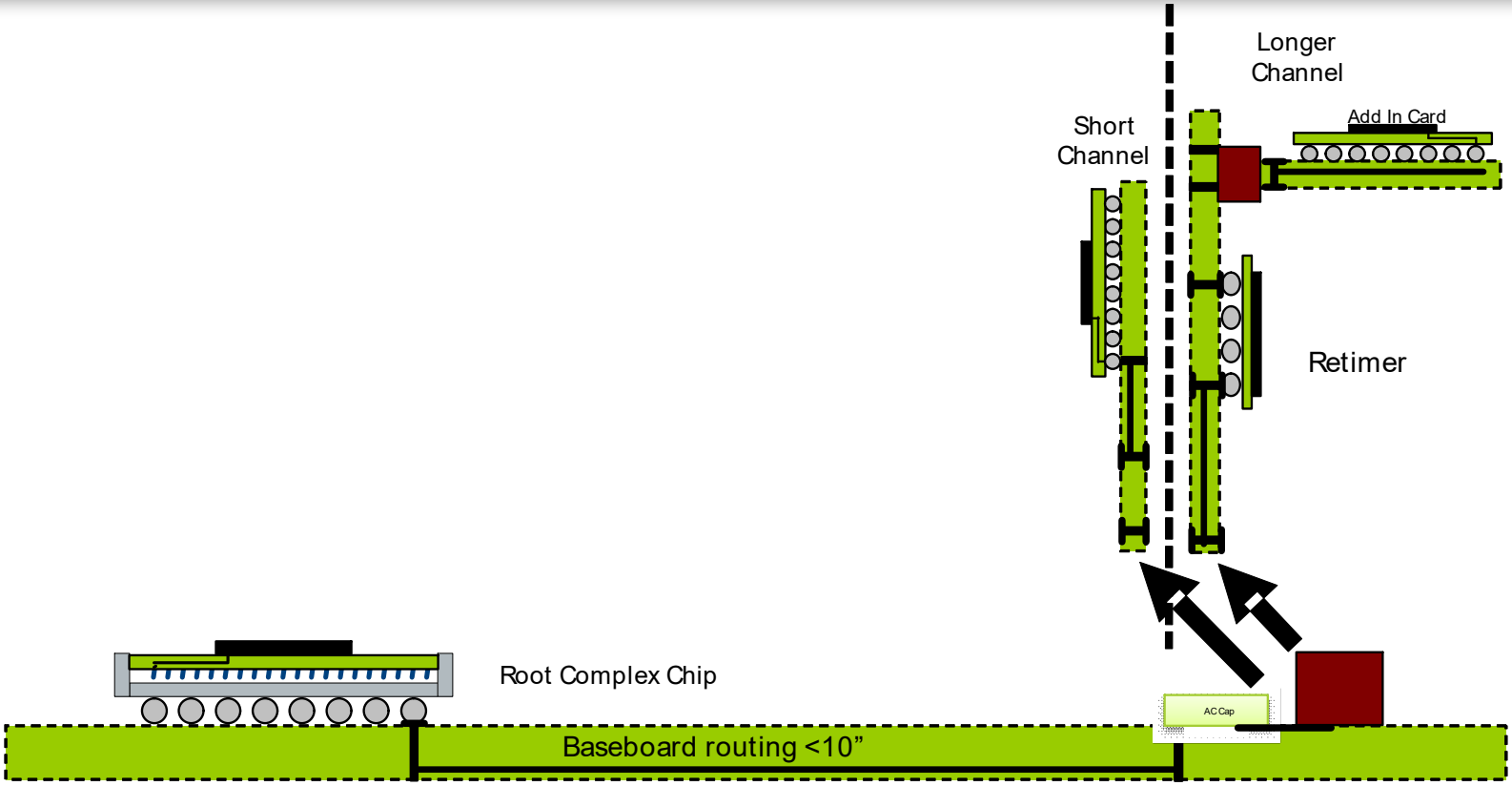


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Back-up

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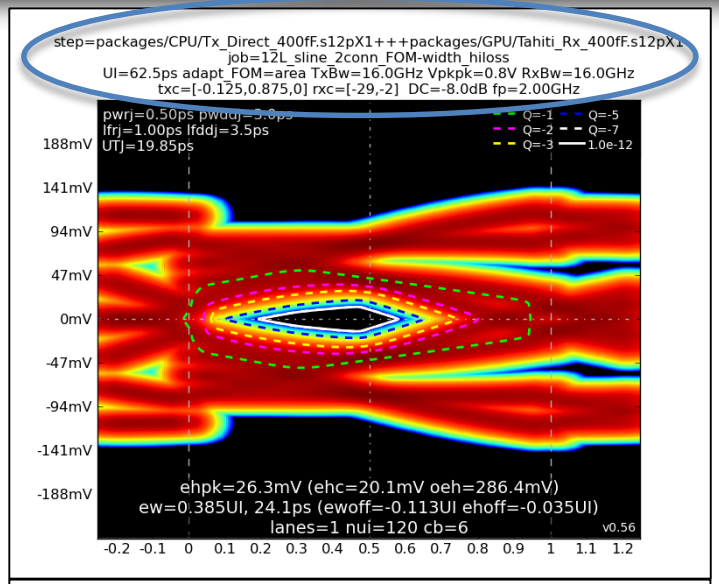
PCI Express 4.0 Channels

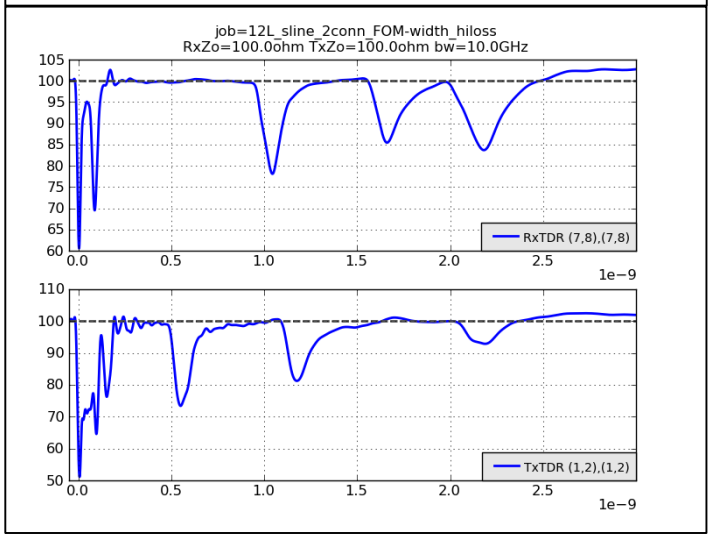


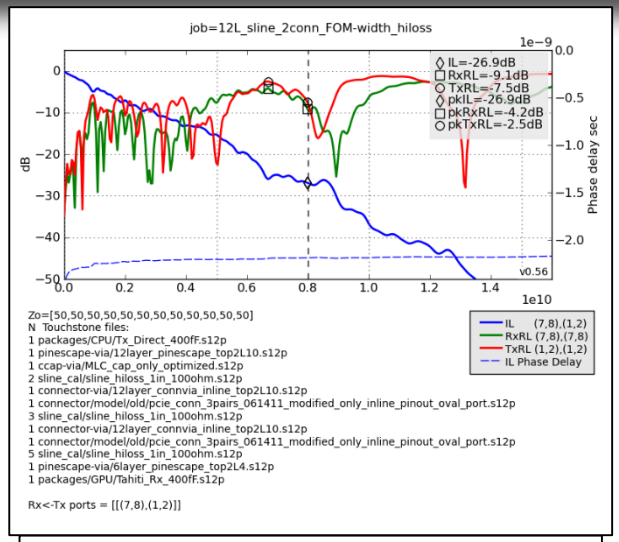
- End to end loss target ~= 28 dB
- Root Package loss ~= 5 dB
- Add-in Card Package loss ~= 3 dB
- Total Add-in Card ~= 8.0 dB
- Connector < 1 dB

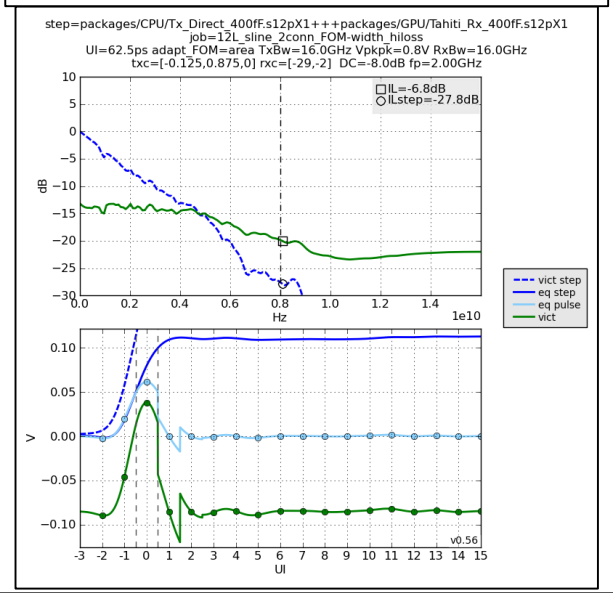
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EQ Tuning – High Loss Two Connector Server





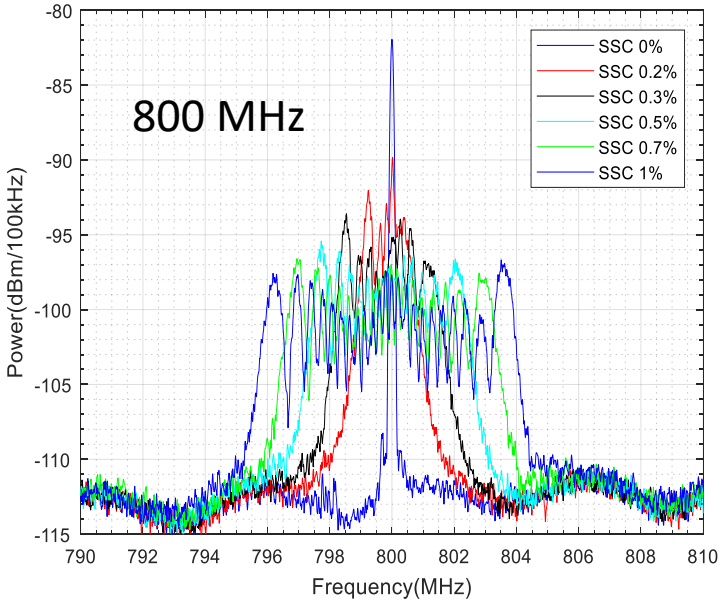




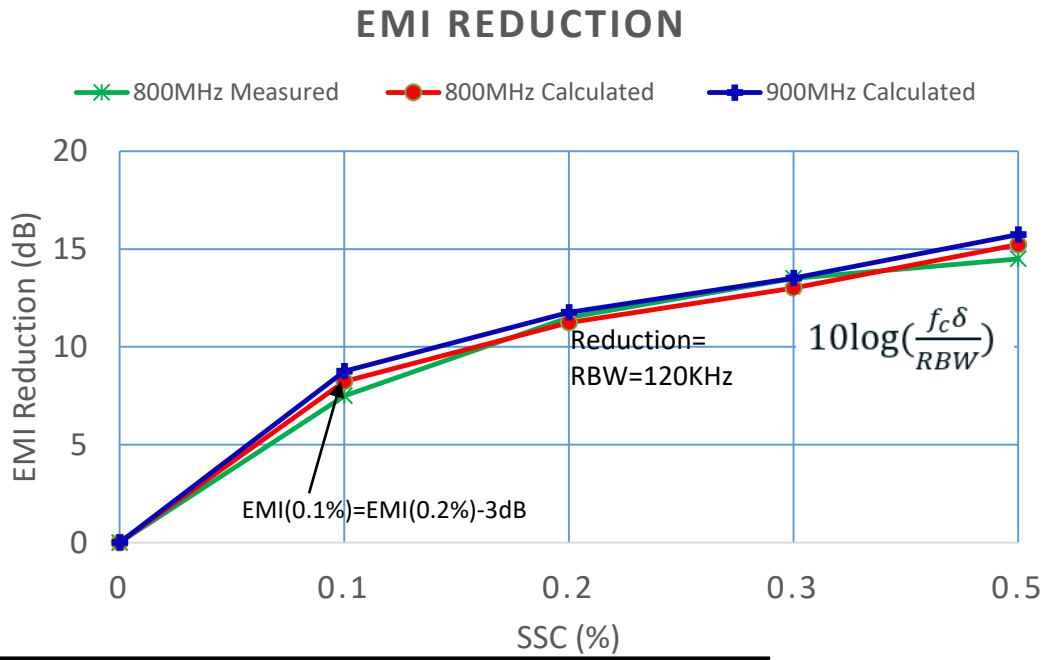
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SRIS – Maximum SSC PPM

- Spectrum analyzer measurement
 - Average detector, 100kHz RBW



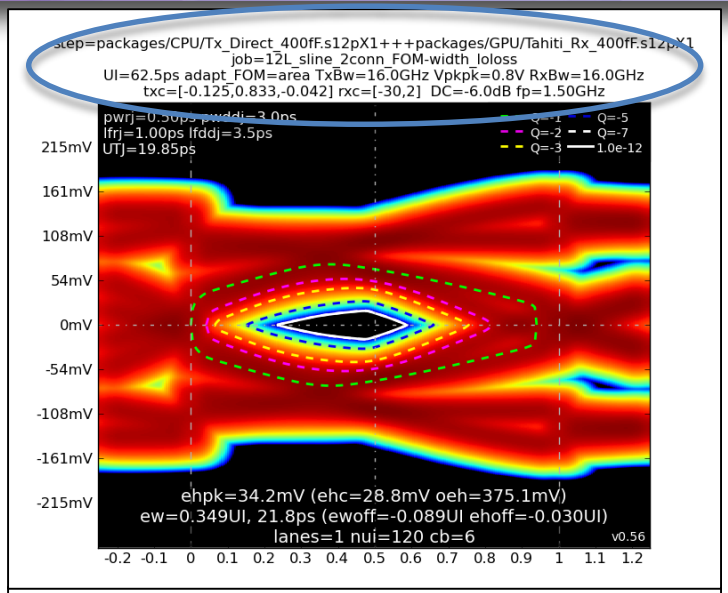
EMI (<1GHz; RBW=100Khz) vs. SSC %
(Measured Data from an Actual SOC)

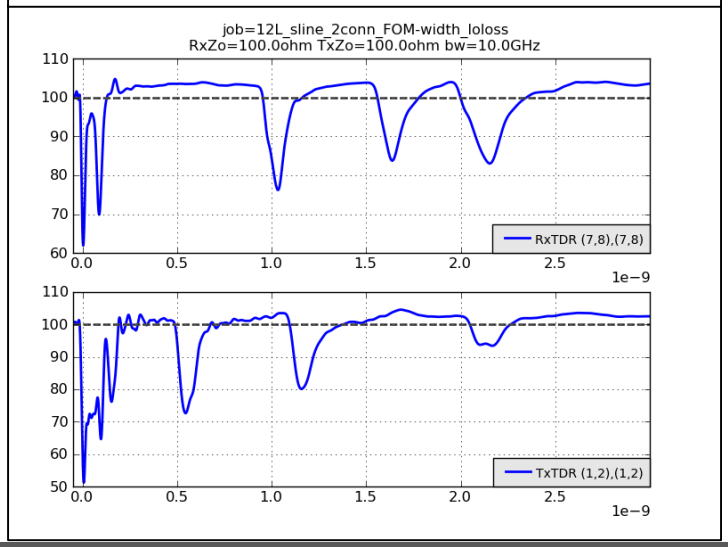


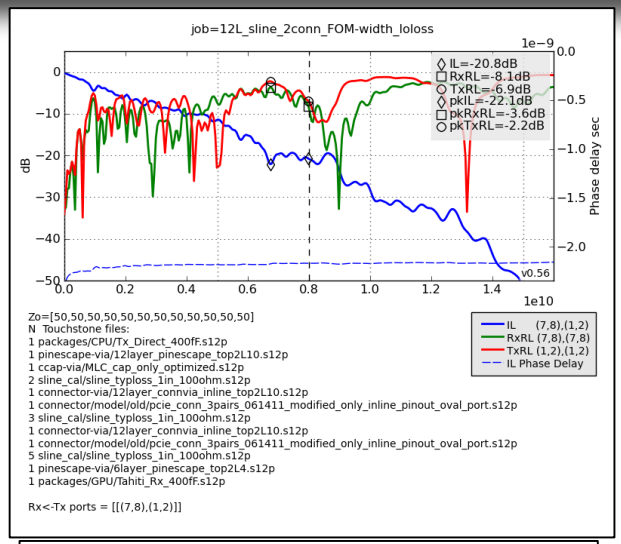
PPM	900MHz EMI Benefit Losses from 0.5%
0.3%	~2dB
0.2%	~4dB
0.1%	~7dB
0%	~15dB

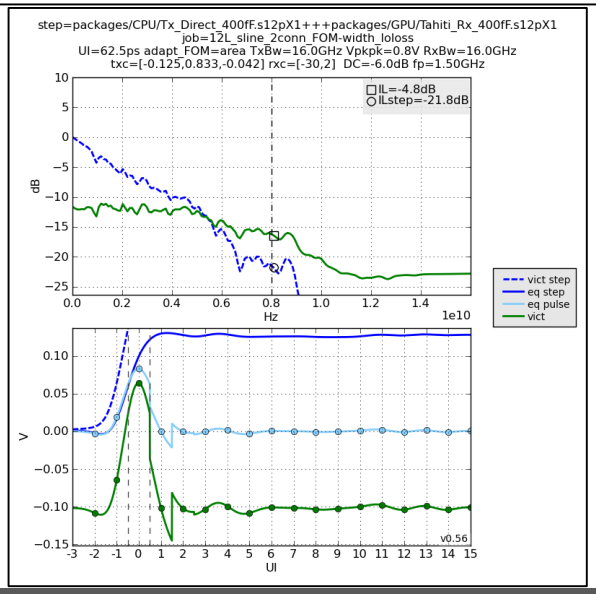
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EQ Tuning – Low Loss Two Connector Server



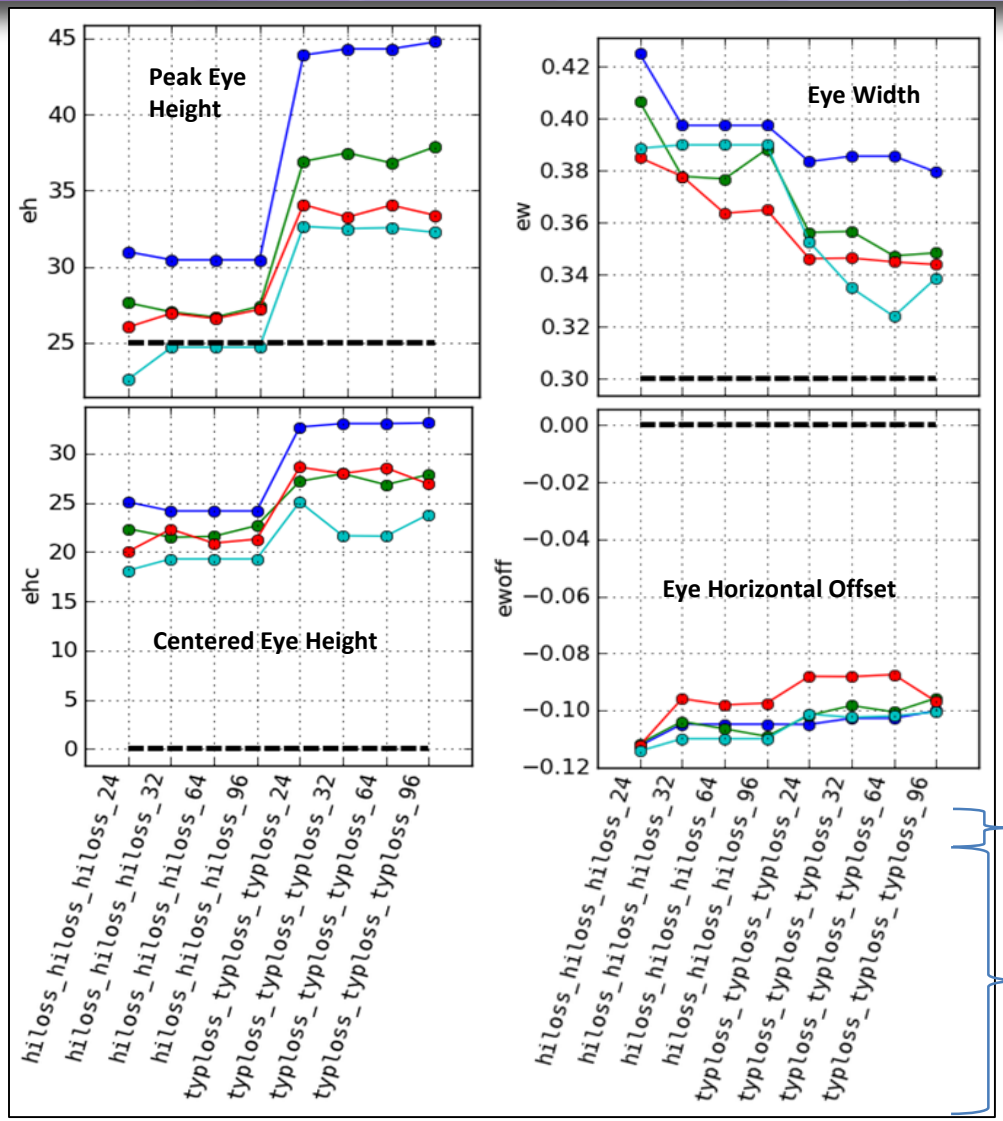


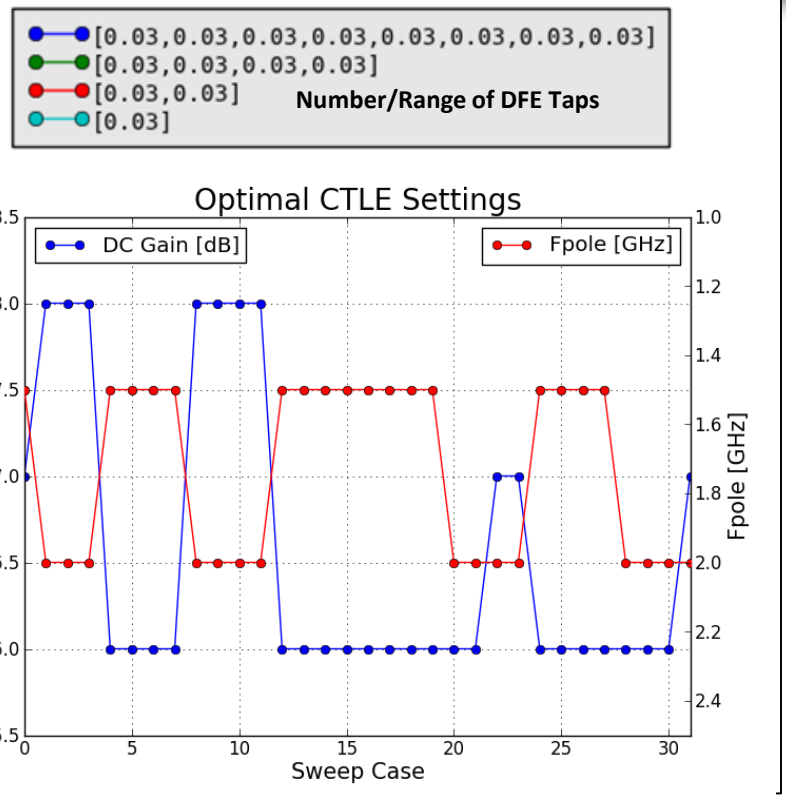




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Equalization Sweep





Tx Tap Resolution
[1/24, 1/32, 1/64, 1/96]

Channel PCB Variation
[Tline1_Tline2_Tline3]

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Waveform Post Processing Tool Requirements

- The test channel is the long Rx calibration channel with the Root reference package
- A step pattern with 256 ones and zeros is captured through the test channel by averaging 128 times on a real time oscilloscope for each preset.
- The channel compliance methodology is run and the TX EQ preset that produced the largest eye area is selected for exact eye height and width calibration.
- The channel compliance methodology is used with the selected TX EQ preset to produce an EH/EW of 15 mV and .3 UI @ E-12 BER by adjusting the Sj and voltage swing at the transmitter output.
- A pattern generator is calibrated to have the same jitter stress levels and Tx Swing as those used in the channel compliance simulations that produced an EH/EW of 15 mV and .3 UI @ E-12 BER at the pattern generator output.
- 2 million unit interval waveforms with compliance pattern are captured at each TX EQ preset at the end of the channel.
- For the preset that gives the largest eye area with the waveform post processing tool the EH and EW @ E-12 BER must match 15 mV and .3 UI within +/- 15%.

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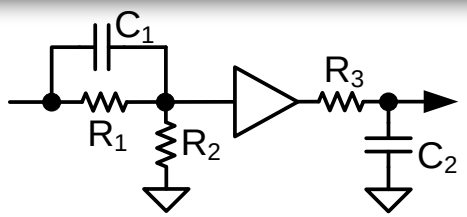
Tx Testing: Base vs. CEM

- **CEM Tx Testing:**
 - End of reference channel waveform post-processed with reference equalizer. Best assessment of silicon-channel interaction.
 - Eye measured at a BER of 1E-12.
 - RJ & DJ gross separation performed at end of reference channel.
 - Eye may be closed at CEM connector for long channel designs.
 - Tx eye test only required to pass with optimal preset.

- **Mainboard Tx Testing:**
 - Non-ideal mainboard reference clock.
 - Suitable for testing commercially available mainboards.
 - Dual-port methodology samples Tx data lane and 100MHz ref clock.

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Receiver Linear Equalizer Pole 1 at 2 GHz



$$H(s) = \frac{sC_1R_1R_2 + R_2}{sC_1R_1R_2 + R_1 + R_2} \cdot \frac{1}{sC_2R_3 + 1}$$

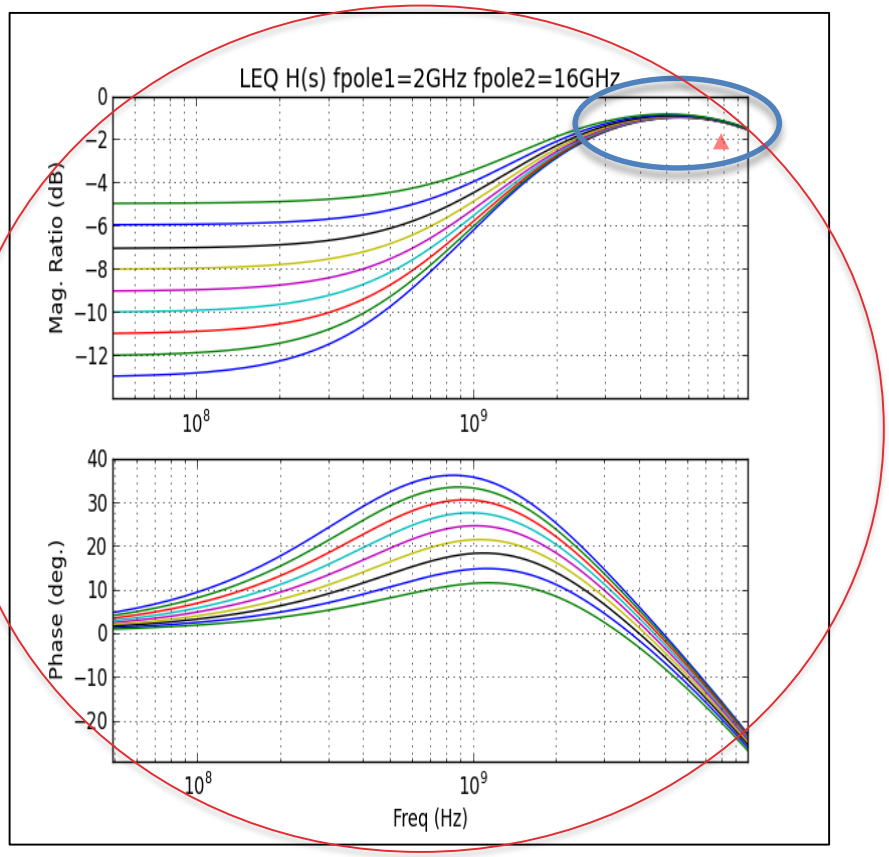
$$H(s) = \frac{R_2}{R_1 + R_2} \cdot \frac{\frac{s}{\omega_Z} + 1}{\frac{s}{\omega_{P1}} + 1} \cdot \frac{1}{\frac{s}{\omega_{P2}} + 1}$$

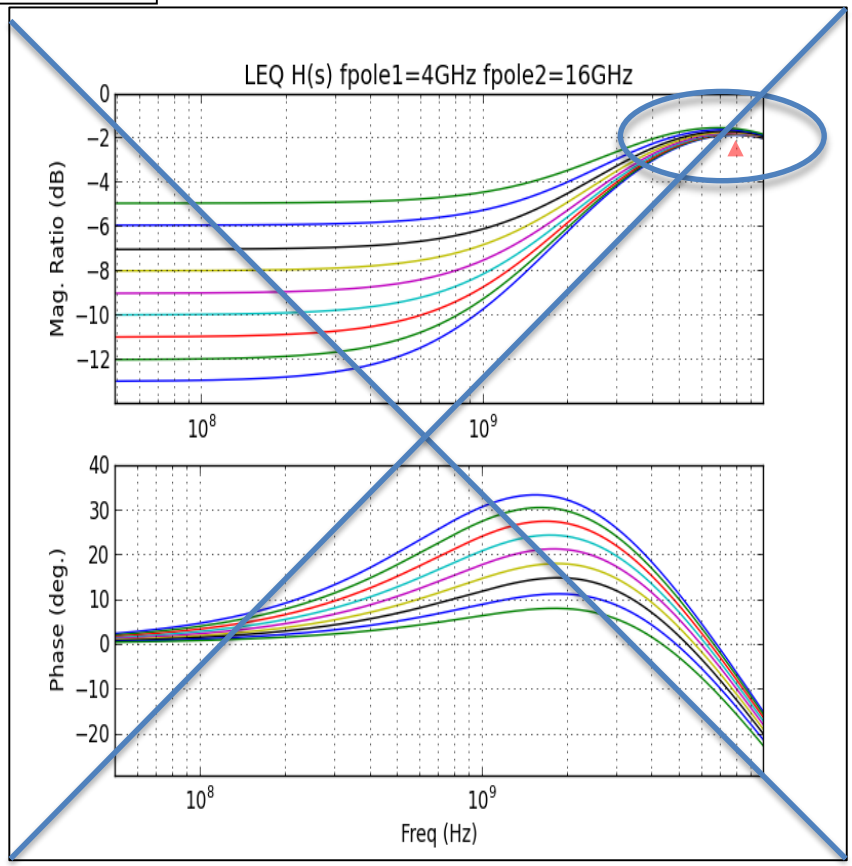
$$G_{DC} = \frac{R_2}{R_1 + R_2}$$

$$\omega_{P1} = \frac{R_1 + R_2}{C_1R_1R_2}$$

$$\omega_Z = \frac{1}{C_1R_1} = G_{DC}\omega_{P1}$$

$$\omega_{P2} = \frac{1}{C_2R_3}$$





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CC Reference Clock Specification (Implementation Trade-off for IR)

Data Rate	CC jitter Limit	Notes
2.5G	108 ps pp	1, 2
5.0G	3.1 ps RMS	1, 2
8.0G	1.0 ps RMS	1, 2
16G	0.5 ps RMS Note that .7 ps RMS is to be used in channel simulations to account for additional noise in a real system.	1,2, 3

Note:

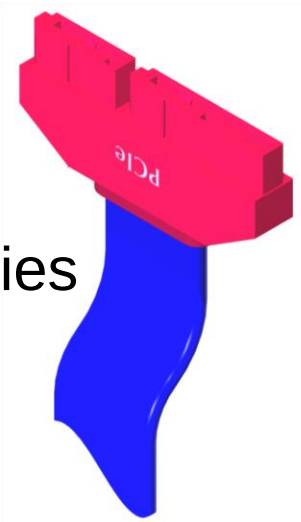
1. The Refclk jitter is measured after applying the filter function in Figure 9-45
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope with a sample rate of 20 GS/s or great. Broadband oscilloscope noise must be minimized in the measurement.
3. For the 16 GT/s CC measurement SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.

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Inexpensive Cabling
Independent Clock + Spread Spectrum (SSC) (SRIS)

- Challenge: PCI Express® (PCIe) spec did not support independent clock with SSC
 - SATA* cable ~ $0.50
 - PCIe cables include reference clock > $1 for equivalent cable
- PCIe base spec 3.0 ECNs approved
 - 1) Requires use of larger elasticity buffer
 - 2) Requires more frequent insertion of SKIP ordered set
 - 3) Requires receiver changes (CDR)
 - 4) Second ECN updates Model CDRs
- SRIS will create a number of new form factor opportunities for PCIe
 - OCuLink*
 - Lower cost external/internal cabled PCIe
 - Next generation of PCI-SIG* cable specification

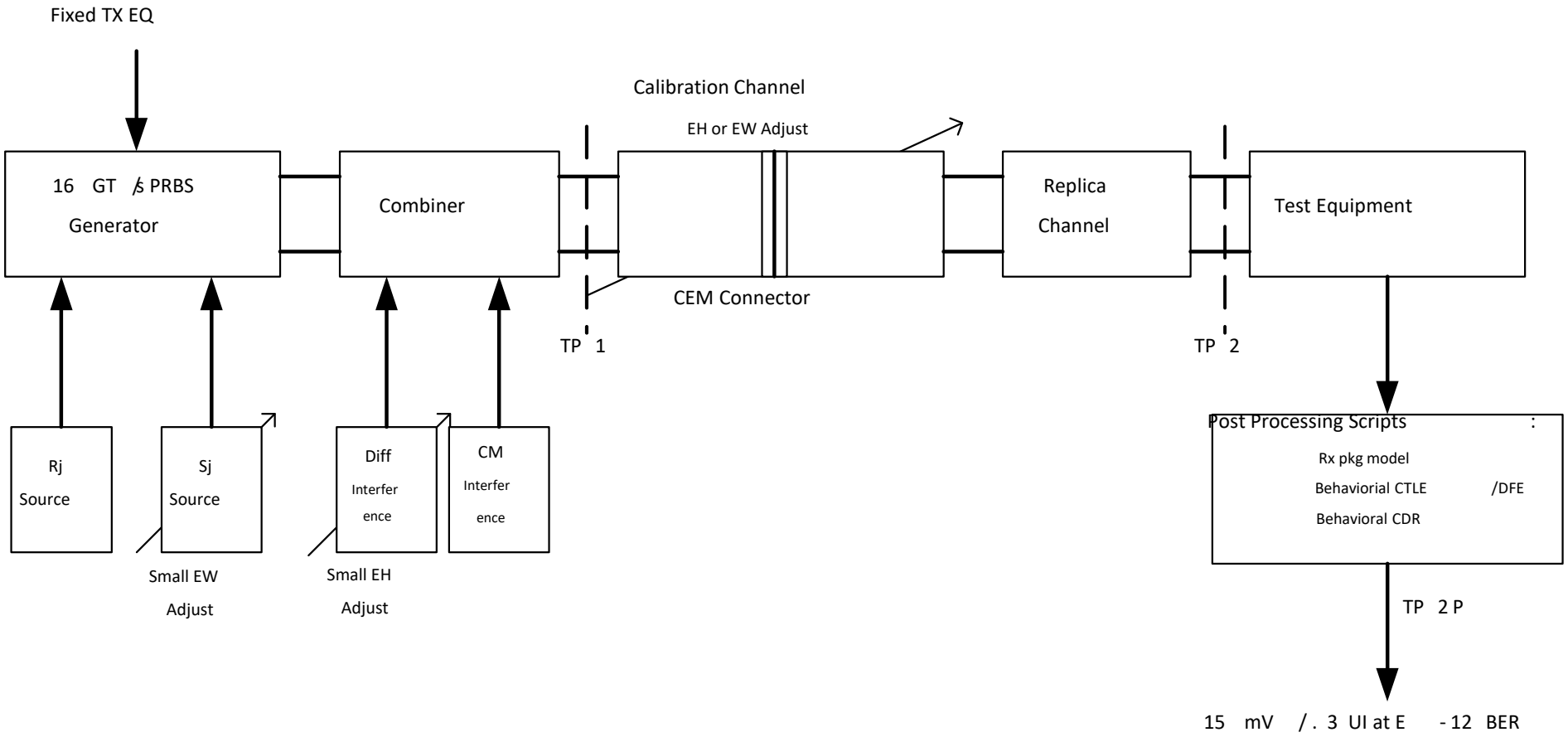
Example of Possible PCIe Cable



Introduce New Terms for Separate Refclk Modes of Operation
5600ppm (New - SRIS) and 600ppm (Existing - SRNS)

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Calibrating Stressed Eye



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Rx Cal Process (1)

- Calibrate the stress values to the nominal values in Rx Cal Details Tables
- Select an initial test channel length that give a loss at TP2P at 8 GHz of 27 dB +/- .5 dB.
- Measure the eye diagram for each TX EQ preset using the nominal TX Eq for the preset +/- .1 dB and select the TX EQ preset that gives the largest eye area.
- For all EH, EW and eye area measurements performed in receiver calibration the A_{DC} in the reference receiver CTLE is varied over its minimum to maximum range in .25 dB steps. This is done to improve repeatability and accuracy in automated Rx calibration software and is only done for stressed eye calibration (not for channel compliance, etc.)
- Increase the calibration channel loss to the next available length/loss and measure the new eye diagram at the selected preset. Continue to increase the length/loss until either the height or width have fallen below the targets in Table 9-9 then the previous calibration channel length/loss is selected. If neither the height or width have fallen below the targets and the TP1 to TP2P loss at 8 GHz has reached 30.0 dB then advance to the next step.
- For the selected calibration channel length/loss, measure the eye diagram for each TX EQ preset and select the preset that gives the largest eye area. Note that this may be a different preset than step 3 due to the length/loss change.

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Rx Cal Process (2)

- **Adjust Sj, DM, and Voltage Swing to make final adjustments to the eye by sweeping them through the following ranges:**
 - Sj – 5 to 10 ps PP.
 - DM – 10 to 25 mV at TP2.
 - Differential Voltage Swing – 720 to 800 mV PP at TP1.
- **If the final Sj value is less then 0.1 UI then the Rj level is reduced so the eye width meets the target eye width with 0.1 UI of 100 MHz Sj.**
- **If there are multiple combinations of Sj, DM, and Voltage Swing that give valid solutions first pick the combination that is closest to the target eye width (18.75 ps). If there are multiple Sj, DM, and Voltage Swing combinations that are equally close to the target eye width then pick the one with Sj closest to nominal. The selected values must give a mean eye height and width (over at least 5 measurements – exact number of measurements needed for stable values will depend on lab set-up and tools) within the following ranges at BER E-12:**
 - Eye height – 15 mV +/- 1.5 mV
 - Eye width – 18.75 ps +/- 0.5 ps

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Rx Cal Details
Differential Noise and SSC Residual

Symbol	Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	Units	Details
$V_{RX-LAUNCH}$	Generator launch voltage	800-1200	800-1200	800-1200	800-1200	mV PP	Note 1
T_{RX-UI}	Unit Interval	400	200	125	62.5	ps	
T_{RX-ST}	Eye width at TP2P	<0.4	<0.32	0.30	0.30	UI	Note 3,4, 10
V_{RX-ST}	Eye height at TP2P	175	100	25	15	mV PP	Note 2,4, 9
$T_{RX-ST-SJ}$	Swept Sj	N/A	N/A	Figure 9-29, Figure 9-30	Figure 9-29, Figure 9-30	UI PP	Note 5, Sec. 9.4.2.2.1 ff.
$T_{RX-ST-RJ}$	Random Jitter	N/A	3.4 (max)	3.0 (max)	1.0 (max)	ps RMS	Note 6,7
$V_{RX-DIFF-INT}$	Differential noise (2.1 GHz)	N/A	N/A	14	14	mV PP	Note 6,7
$V_{RX-CM-INT}$	Common mode noise	150	150	150	150	mV PP	Note 8
$V_{SSC-RES}$	SSC Residual	N/A	75	N/A	500	ps PP	Note 11

Note 11: Applied for CC testing only as triangular frequency modulation with a frequency between 30 and 33 KHz.

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Package Evaluation Process

- **Some packages are allowed to have insertion loss and/or cross-talk that exceed the reference packages**
- **Actual package performance must be evaluated**
- **Evaluation performed by running set of channel compliance simulations with reference channels replacing one reference package with package under evaluation**
- **Package with worse performance than reference must use actual package in channel compliance simulation and may use actual package in receiver calibration**

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CEM Channel Decisions

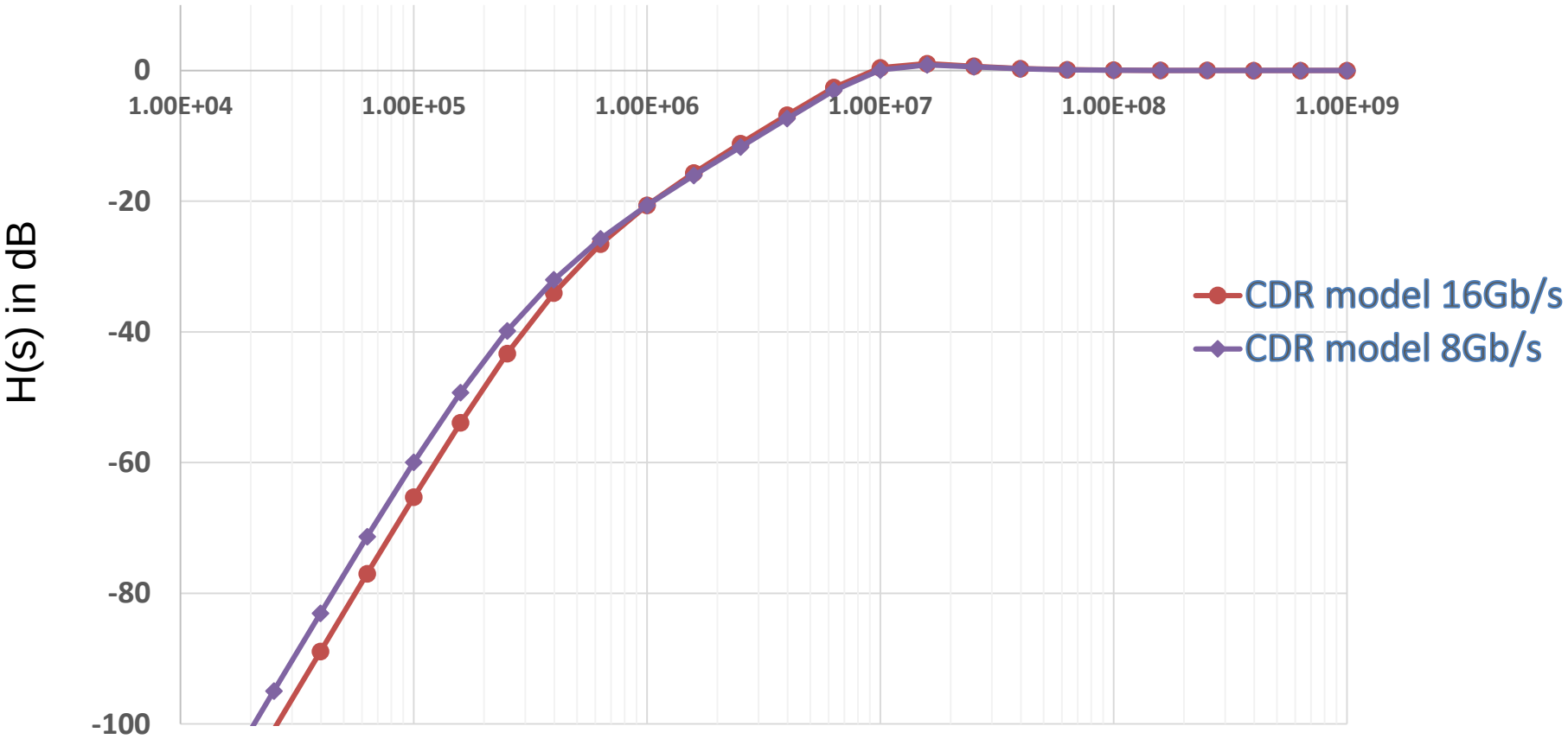
- **AIC Frequency Domain Loss Limit – 8 dB at 8 GHz**
 - An AIC ILpad-to-finger loss spec provides flexibility for implementation
 - Tradeoff package loss for PCB length, or pursue lower loss materials, etc.
 - Max trace length of 4” still possible with package improvement and/or lower loss materials

Loss budgets for channel max IL = -28dB:

	Option 1		Option 2		Selected Limits	
Channel Max IL: -28dB	aic	mainboard	aic-1	mainboard-1	aic-2	mainboard-2
loss budget (dB)	9.6	18.4	8.6	19.4	8.0	20.0
pkg loss (dB)	3	5	3	5	3	5
via loss (dB)	1	1	1	1	1	1
CEM Connector (dB)	----	1	----	1	----	1
PCB Etch IL (dB)	5.6	11.4	4.6	12.4	4.0	13.8
etch Length @ -1.4dB/inch	4	8.1	3.3	8.9	2.8	9.8
etch Length @ -1.1dB/inch	5.1	10.4	4.2	11.3	3.6	12.5
etch Length @ -0.8dB/inch	7.0	14.3	5.8	15.5	5.0	17.2

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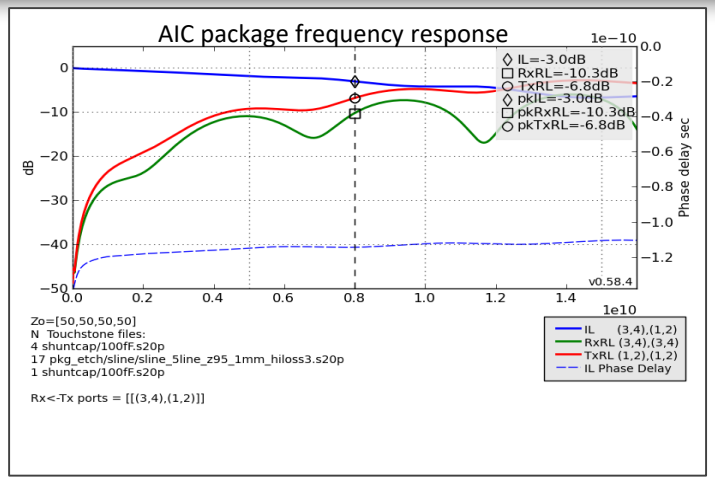
Updated SRIS Model CDRs

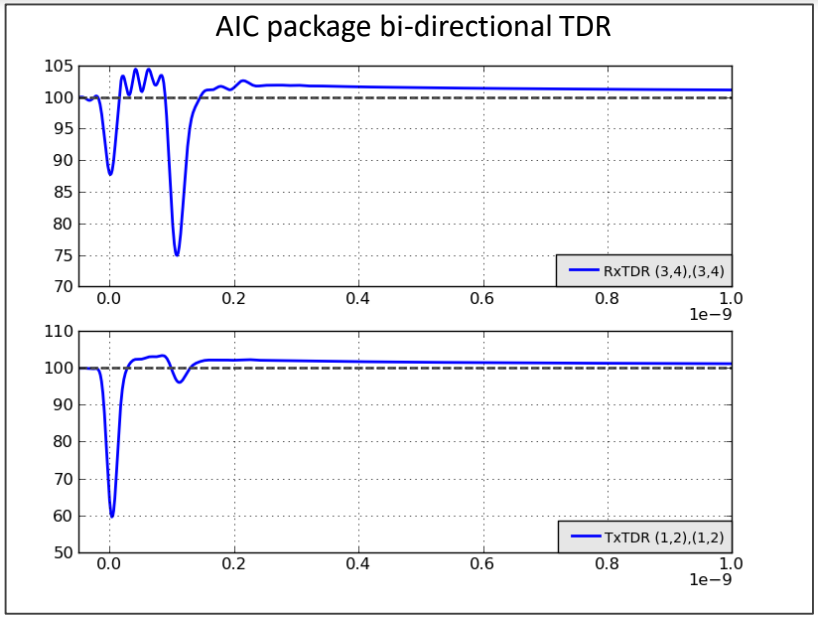


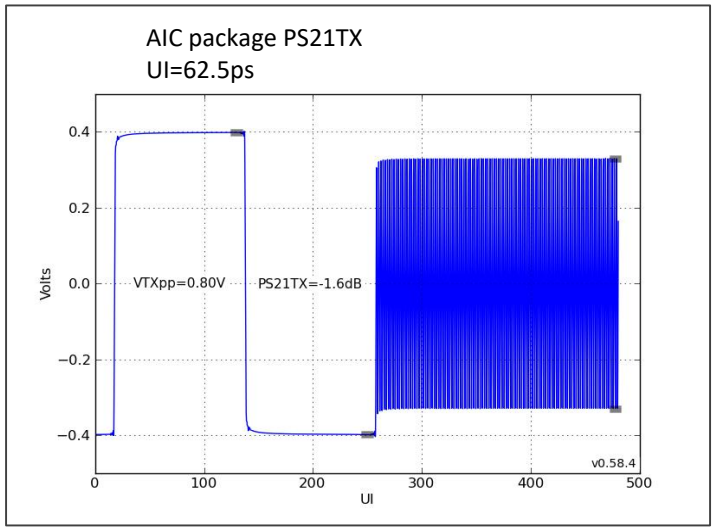
More Rejection Was Needed at LF for Tx and Reference Clock Analysis

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AIC Tx Package Loss Update







- **Base Spec AIC Loss:**
 - Informative IL limit = -3dB
 - Normative for Captive Channel Support
 - Tx-AIC-DEVICE PS21TX
 - Vendor must ensure Form Factor limits can be met

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